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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,173	04/22/2004	Syotaro Ono	252311US2S	6045

22850 7590 06/16/2006

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,173	ONO ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8 and 10* is/are pending in the application.

4a) Of the above claim(s) *9 and 11-18* is/are withdrawn from consideration.

5)☒ Claim(s) *8* is/are allowed.

6)☒ Claim(s) *1-4,6 and 10* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/12/06 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1,4,6, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over SCHUTTEN ET AL. (4,541,001) in view of BULUCEA ET AL. (5,072,266).

Schutten et al. discloses a semiconductor device comprising a first semiconductor (DRAIN) region 4a of a first conductivity (n) type; a second semiconductor (BASE) region 54a of a second conductivity (p) type formed on the first semiconductor (DRAIN) region 4a; a third semiconductor (SOURCE) region 50a of the first conductivity (n) type

formed on a part of the second semiconductor (BASE) region 54a, the first to third semiconductor regions being formed into a MOS field-effect transistor; a fifth semiconductor region 118 of the second conductivity (p) type formed on a part of the second semiconductor (BASE) region 54a, the fifth semiconductor region 118 having an impurity concentration (p+) higher than an impurity concentration of the second semiconductor (BASE) region 54a; and a source electrode 64a formed on the fifth semiconductor region 118 and the third semiconductor (SOURCE) region 50a; a trench 12 formed to range from a surface of the third semiconductor (SOURCE) region 50a to the third semiconductor (SOURCE) region 50a and the second semiconductor (BASE) region 54a, the trench 12 penetrating the third semiconductor (SOURCE) region 50a, the trench 12 having no second semiconductor (BASE) region 54a under its bottom surface; a gate insulating film 30,32 formed on both facing side surfaces of the trench 12; first 34a and second 36a gate electrodes formed on the gate insulating film 30,32 and opposed to the facing side surfaces of the trench 12, the first 34a and second 36a gate electrodes being separated from each other; the separated first 34a and second 36a gate electrodes including, in a cross sectional cut in a depth direction of the trench 12 and including the first 34a and second 36a gate electrodes, at least one portion to which the first 34a and second 36a gate electrodes are not connected; and a floating electrode first conductive material 40 formed between the first 34a and second 36a gate electrodes on the side surfaces of the trench 12, with an insulating film 38 intervened

between the first conductive material 40 and the first 34a and second 36a gate electrodes. Note figure 7, column 7 lines 63-69, and column 8 lines 1-21 of Schutten et al. Schutten et al. does not disclose that a depth of the trench is shorter than a depth of a deepest bottom portion of the second semiconductor (BASE) region. However, Bulucea et al. discloses a semiconductor device comprising a second semiconductor (BASE) region 27 of a second conductivity (p) type; a third semiconductor (SOURCE) region 28 of a first conductivity (n) type formed on a part of the second semiconductor (BASE) region 27; a trench 29 formed to range from a surface of the third semiconductor (SOURCE) region 28 to the third semiconductor (SOURCE) region 28 and the second semiconductor (BASE) region 27, the trench 29 penetrating the third semiconductor (SOURCE) region 28, the trench 29 having no second semiconductor (BASE) region 27 under its bottom surface; wherein a depth of the trench 29 is shorter than a depth of a deepest bottom portion 27c of the second semiconductor (BASE) region 27. Note figure 8, column 6 lines 27-61, and especially column 7 lines 5-9 and 14-20 of Bulucea et al., explaining that an important advantage accrues when deep bottom BASE portion 27c is deeper than the trench 29. The deep bottom BASE forces breakdown, when it occurs, away from the trench 29 and into the body of the BASE region, making it free of high current concentrations and relatively stable, with good suppression of hot current. Therefore, it would have been obvious to a person having skill in the art to augment Schutten et al.'s semiconductor device with the trench having

a depth that is shorter than a depth of a deepest bottom portion of a second semiconductor (BASE) region such as taught by Bulucea et al. in order to force breakdown into the bulk region of the device to thus provide a device that is free of high current concentrations and relatively stable, with good suppression of hot current.

B. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over SCHUTTEN ET AL. (4,541,001) in view of BULUCEA ET AL. (5,072,266), as applied to claim 1, above, and further in view of HSHIEH ET AL. (5,929,481).

Schutten et al. and Bulucea et al. teach a semiconductor device having all the limitations of claims 2 and 3 except a fourth semiconductor region of the first conductivity type arranged apart in boundary regions of the first semiconductor (DRAIN) region and the second semiconductor (BASE) region and formed between the bottom surface of the trench and the first semiconductor (DRAIN) region, the fourth semiconductor region having an impurity concentration higher than an impurity concentration of the first semiconductor (DRAIN) region. Note figure 7, column 7 lines 63-69, and column 8 lines 1-21 of Schutten et al., and figure 8, column 6 lines 27-61, and column 7 lines 5-9 and 14-20 of Bulucea et al. However, Hshieh et al. discloses semiconductor device with a fourth semiconductor region 70 of the first conductivity (n) type arranged apart in boundary regions of a first semiconductor (DRAIN) region 54 and a second semiconductor (BASE) region 56 and formed between the bottom surface of a trench and the first semiconductor (DRAIN) region 54, the fourth semiconductor region

70 having an impurity concentration higher than an impurity concentration of the first semiconductor (DRAIN) region 54. Note figure 2 and column 4 lines 31-46 of Hshieh et al. Hshieh et al. specifically teaches, note column 4 lines 37-40, that said fourth semiconductor region 70 having said higher impurity concentration eliminates parasitic JFET effect in devices of this type Therefore, it would have been obvious to a person having skill in the art to augment Schutten et al. and Bulucea et al.'s semiconductor device with the fourth semiconductor region of the first conductivity type arranged apart in boundary regions of the first semiconductor (DRAIN) region and the second semiconductor (BASE) region and formed between the bottom surface of the trench and the first semiconductor (DRAIN) region, the fourth semiconductor region having an impurity concentration higher than an impurity concentration of the first semiconductor (DRAIN) region, such as taught by Hshieh et al. in order to eliminate parasitic JFET effect in order to allow increased cell density and thus higher current from a smaller device.

Response to Arguments

2. Applicant's arguments with respect to claims 1-4,6, and 10 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

3. Claim 8 is allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a combination including all the limitations of claim 1 device, as claimed 11/28/05 and rejected as anticipated by Ueno, as well as being anticipated by Takahashi et al., said limitations being combined with the limitations of claims 7 and 8.

4. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

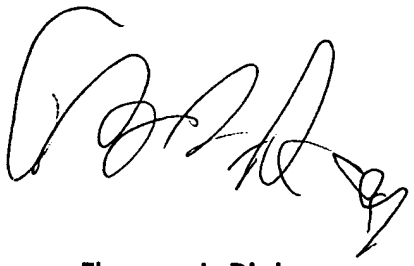
Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
06/06